Integrated Circuit Systems, Inc.

ICS87008I

LOW SKEW, 1-TO-8 DIFFERENTIAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS87008I is a low skew, 1:8 LVCMOS/LVTTL Clock Generator and is a member of the HiPerClockS™ family of High Performance Clock Solutions. The device has 2 banks of 4 outputs and each bank can be independently selected for ÷1 or ÷2 frequency operation. Each bank also has its own power supply pins so that the banks can operate at the following different voltage levels: 3.3V, 2.5V, and 1.8V. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

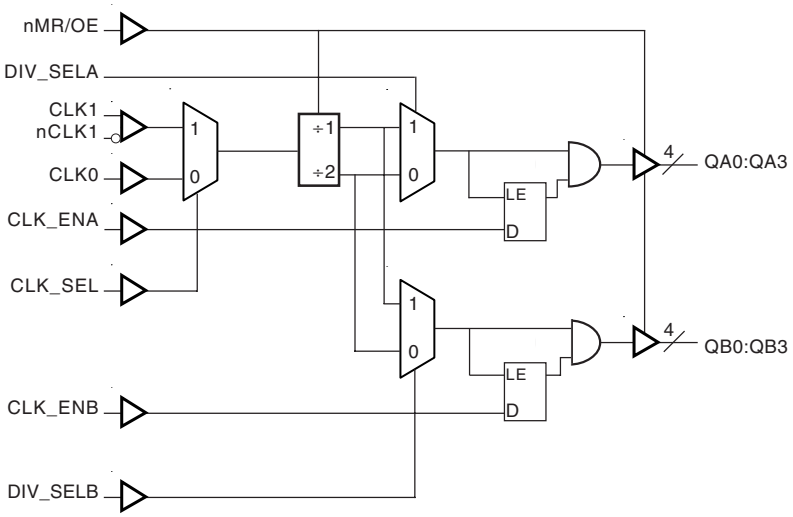
The divide select inputs, DIV_SELA and DIV_SELB, control the output frequency of each bank. The output banks can be independently selected for ÷1 or ÷2 operation. The bank enable inputs, CLK_ENA and CLK_ENB, support enabling and disabling each bank of outputs individually. The CLK_ENA and CLK_ENB circuitry has a synchronizer to prevent runt pulses when enabling or disabling the clock outputs. The master reset input, nMR/OE, resets the ÷1/÷2 flip flops and also controls the active and high impedance states of all outputs. This pin has an internal pull-up resistor and is normally used only for test purposes or in systems which use low power modes.

The ICS87008I is characterized to operate with the core at 3.3V or 2.5V and the banks at 3.3V, 2.5V, or 1.8V. Guaranteed bank, output, and part-to-part skew characteristics make the 87008I ideal for those clock applications demanding well-defined performance and repeatability.

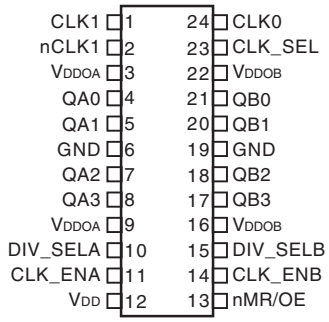
FEATURES

- Eight LVCMOS/LVTTL outputs (2 banks of 4 outputs)
- Selectable differential CLK1, nCLK1 or LVCMOS clock input
- CLK1, nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK0 supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Independent bank control for ÷1 or ÷2 operation
- Glitchless, asynchronous clock enable/disable
- Output skew: 105ps (maximum) @ 3.3V core/3.3V output
- Bank skew: 70ps (maximum) @ 3.3V core/3.3V output
- 3.3V or 2.5V core/3.3V, 2.5V, or 1.8V output operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS87008I
24-Lead TSSOP
4.4mm x 7.8mm x 0.92mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK1	Input	Pulldown	Non-inverting differential clock input.
2	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
3, 9	V_{DDOA}	Power		Output Bank A supply pins.
4, 5, 7, 8	QA0, QA1, QA2, QA3	Output		Bank A outputs. LVCMOS / LVTTL interface levels.
6, 19	GND	Power		Supply ground.
10	DIV_SELA	Input	Pullup	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
11	CLK_ENA	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels.
12	V_{DD}	Power		Power supply pin.
13	nMR/OE	Input	Pullup	Master reset. When LOW, resets the ÷1/÷2 flip flops and sets the outputs to high impedance. LVCMOS / LVTTL interface levels.
14	CLK_ENB	Input	Pullup	Output enable for Bank B outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels.
15	DIV_SELB	Input	Pullup	Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels..
16, 22	V_{DDOB}	Power		Output Bank B supply pins.
17, 18, 20, 21	QB3, QB2, QB1, QB0	Output		Bank B outputs. LVCMOS / LVTTL interface levels.
23	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
24	CLK0	Input	Pulldown	LVCMOS / LVTTL clock input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDOx} = 3.465V; NOTE 1			18	pF
		V_{DD}, V_{DDOx} = 2.625V; NOTE 1			20	pF
		V_{DD} = 3.465, V_{DDOx} = 2.625V; NOTE 1			20	pF
		V_{DD} = 3.465, V_{DDOx} = 1.89V; NOTE 1			30	pF
		V_{DD} = 2.625, V_{DDOx} = 1.89V; NOTE 1			20	pF
R_{OUT}	Output Impedance			7		Ω

NOTE 1: V_{DDOx} denotes V_{DDOA} and V_{DDOB}.

TABLE 3. FUNCTION TABLE

Inputs			Outputs	
nMR/OE	CLK_ENx	DIV_SELx	Bank X	Qx Frequency
0	X	X	Hi Z	N/A
1	1	0	Active	fIN/2
1	1	1	Active	fIN
1	0	X	Low	N/A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Power Supply Current				54	mA
I_{DDOA}, I_{DDOB}	Output Supply Current; NOTE 2				6.5	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, CLK_ENA, CLK_ENB, nMR/OE, CLK_SEL		2		V_{DD} + 0.3	V
		CLK0		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, CLK_ENA, CLK_ENB, nMR/OE, CLK_SEL		-0.3		0.8	V
		CLK0		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, CLK_ENA, CLK_ENB, nMR/OE	V_{DD} = V_{IN} = 3.465V, V_{DD} = V_{IN} = 2.625V			5	µA
		CLK0, CLK_SEL	V_{DD} = V_{IN} = 3.465V, V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, CLK_ENA, CLK_ENB, nMR/OE	V_{DD} = 3.465V, V_{IN} = 0V V_{DD} = 2.625V, V_{IN} = 0V	-150			µA
		CLK0, CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDOx} = 3.3V ± 5%; NOTE 2	2.6			V
			V_{DDOx} = 2.5V ± 5%; NOTE 2	1.8			V
			V_{DDOx} = 1.8V ± 5%; NOTE 2	1.5			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDOx} = 3.3V ± 5%; NOTE 2			0.5	V
			V_{DDOx} = 2.5V ± 5%; NOTE 2			0.5	V
			V_{DDOx} = 1.8V ± 5%; NOTE 2			0.4	V
I_{OZL}	Output Tristate Current Low			-5			µA
I_{OZH}	Output Tristate Current High					5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDOX}/2. See Parameter Measurement Information, Output Load Test Circuits.
NOTE 2: V_{DDOx} denotes V_{DDOA}, and V_{DDOB}.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = V_{DD} = 3.3V±5% OR 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK1	V_{IN} = V_{DD} = 3.465V, V_{IN} = V_{DD} = 2.625V			5	µA
		CLK1	V_{IN} = V_{DD} = 3.465V, V_{IN} = V_{DD} = 2.625V			150	µA
I_{IL}	Input Low Current	nCLK1	V_{IN} = 0V, V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V	-150			µA
		CLK1	V_{IN} = 0V, V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK1, nCLK1 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDOx} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		1.9	3.5	5.1	ns
		CLK1, nCLK1; NOTE 1B		3.0	3.7	4.5	ns
*t*sk(b)	Bank Skew; NOTE 2, 6					70	ps
*t*sk(o)	Output Skew; NOTE 3, 6					105	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					650	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		1100	ps
odc	Output Duty Cycle		f ≤ 133MHz	45		55	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz using CLK1, nCLK1 unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDOx} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		2.0	3.8	5.5	ns
		CLK1, nCLK1; NOTE 1B		3	4	5	ns
*t*sk(b)	Bank Skew; NOTE 2, 6					35	ps
*t*sk(o)	Output Skew; NOTE 3, 6					130	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					1	ns
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		1000	ps
odc	Output Duty Cycle		f ≤ 125MHz	45		55	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz using CLK1, nCLK1 unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOx} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		2.25	3.6	5.0	ns
		CLK1, nCLK1; NOTE 1B		3.1	3.8	4.4	ns
*t*sk(b)	Bank Skew; NOTE 2, 6					60	ps
*t*sk(o)	Output Skew; NOTE 3, 6					130	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					900	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	290		950	ps
odc	Output Duty Cycle		f ≤ 133MHz	45		55	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz using CLK1, nCLK1 unless noted otherwise.
NOTE 1A: Measured from the V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 1B: Measured from the differential input crossing point to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5D. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOx} = 1.8V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		3.0	4.5	4.9	ns
		CLK1, nCLK1; NOTE 1B		3.3	4.1	5.0	ns
*t*sk(b)	Bank Skew; NOTE 2, 6					55	ps
*t*sk(o)	Output Skew; NOTE 3, 6					150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					1.1	ns
t_R / t_F	Output Rise/Fall Time		20% to 80%	280		850	ps
odc	Output Duty Cycle		f ≤ 133MHz	45		55	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

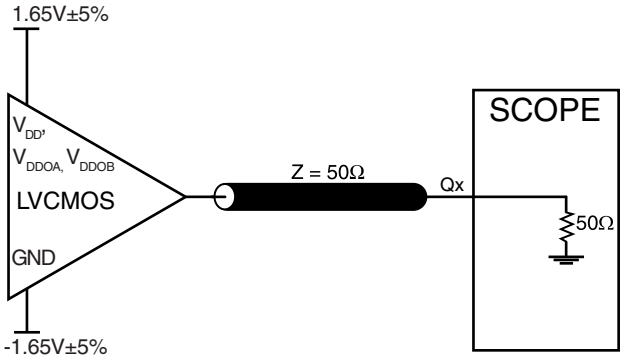
All parameters measured at 250MHz using CLK1, nCLK1 unless noted otherwise.
NOTE 1A: Measured from the V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 1B: Measured from the differential input crossing point to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5E. AC CHARACTERISTICS, V_{DD} = 2.5V±5%, V_{DDOx} = 1.8V±5%, T_A = -40°C TO 85°C

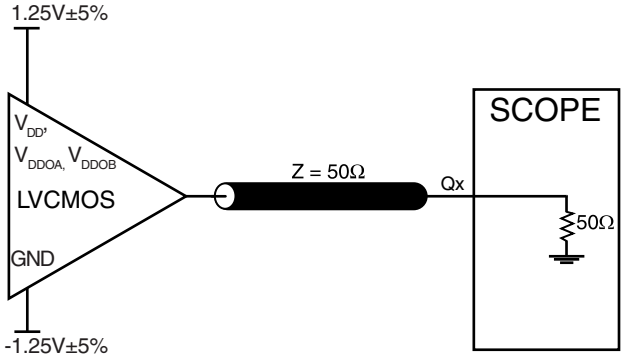
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		2.6	4.1	5.6	ns
		CLK1, nCLK1; NOTE 1B		3.3	4.4	5.4	ns
*t*sk(b)	Bank Skew; NOTE 2, 6					45	ps
*t*sk(o)	Output Skew; NOTE 3, 6					150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					1.2	ns
t_R / t_F	Output Rise/Fall Time		20% to 80%	325		900	ps
odc	Output Duty Cycle		f ≤ 100MHz	45		55	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz using CLK1, nCLK1 unless noted otherwise.
NOTE 1A: Measured from the V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 1B: Measured from the differential input crossing point to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

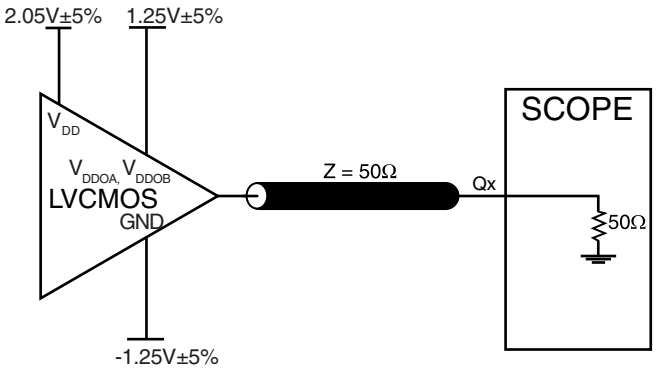
PARAMETER MEASUREMENT INFORMATION



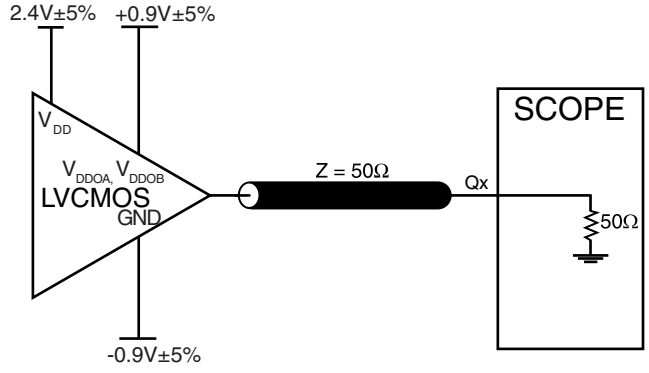
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



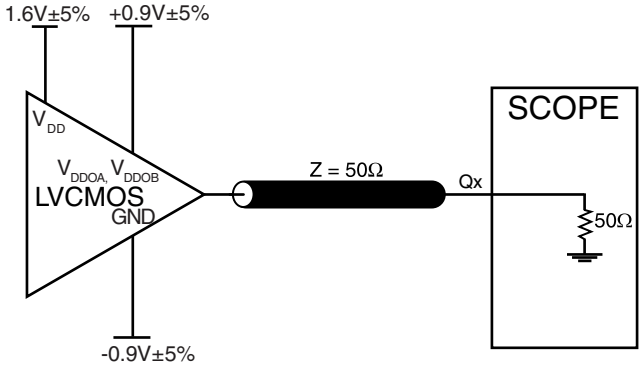
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



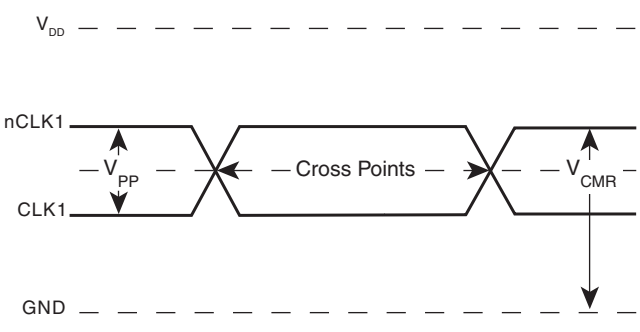
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



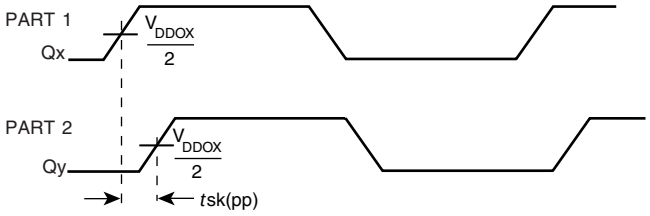
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



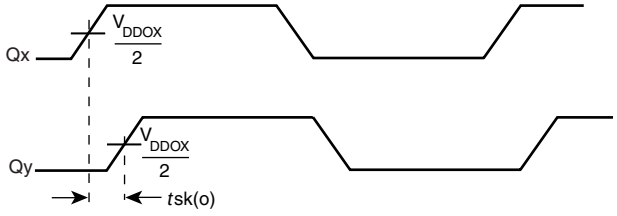
2.5V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



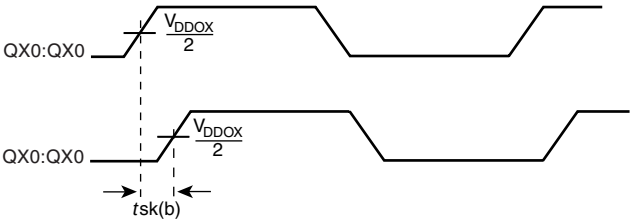
DIFFERENTIAL INPUT LEVEL



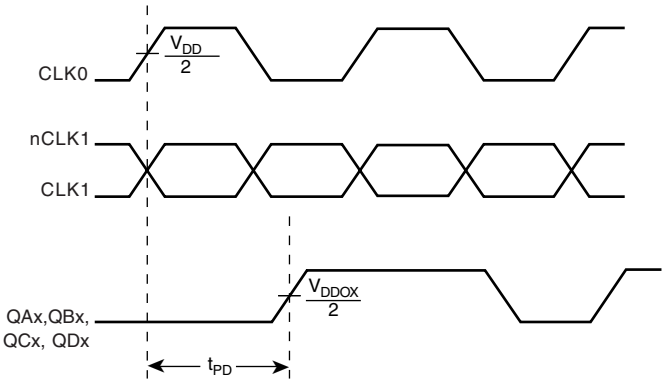
PART-TO-PART SKEW



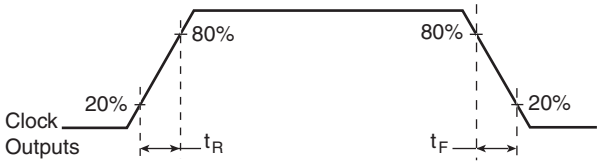
OUTPUT SKEW



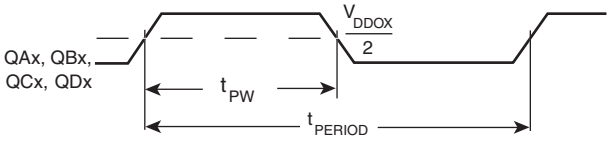
BANK SKEW (where X denotes outputs in the same bank)



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

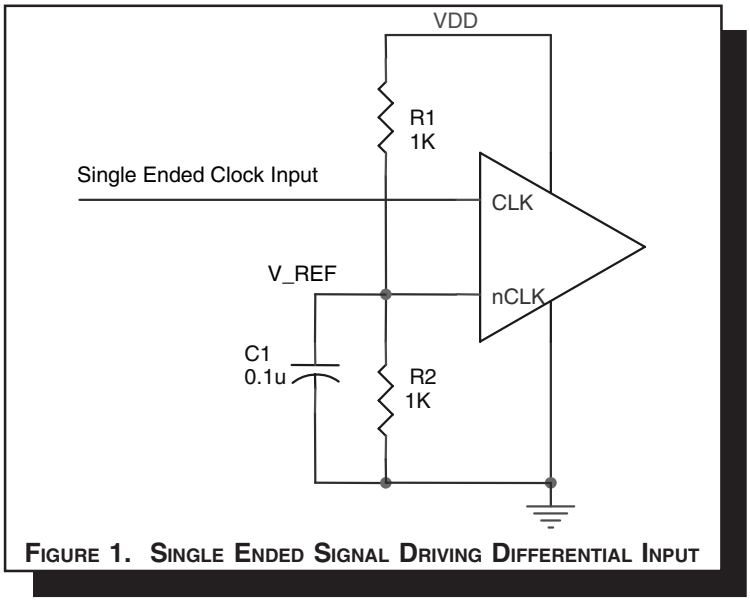


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CLK/nCLK INPUT:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

PCLK/nPCLK INPUT:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

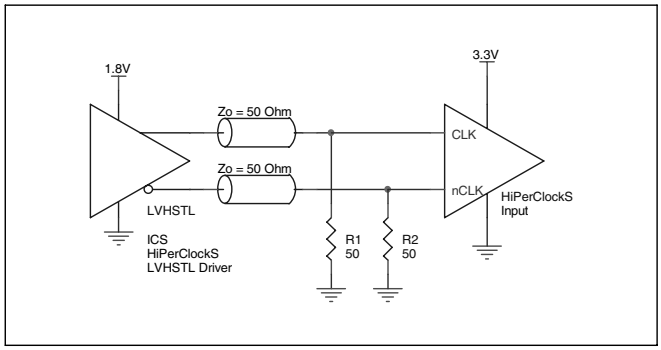


FIGURE 2A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

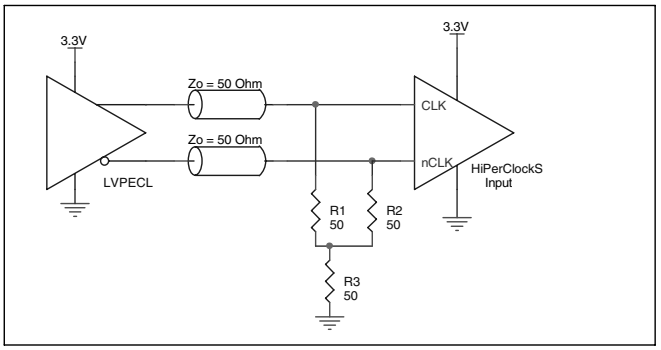


FIGURE 2B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

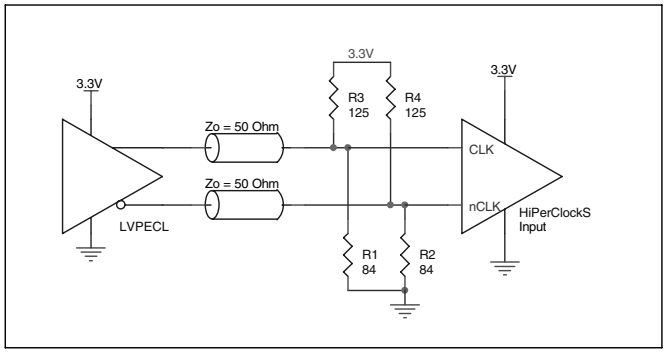


FIGURE 2C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

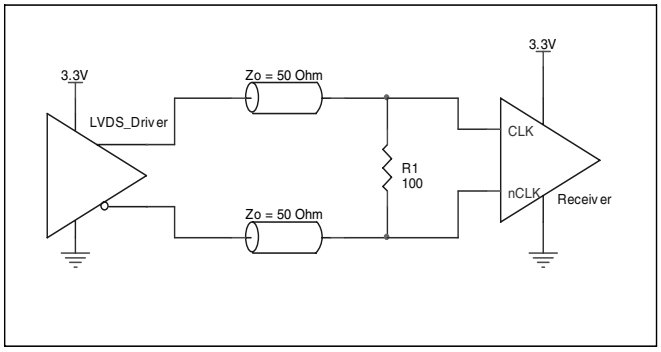


FIGURE 2D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

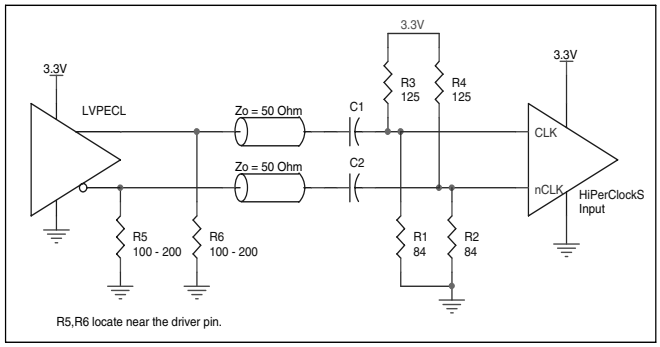


FIGURE 2E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

TRANSISTOR COUNT

The transistor count for ICS87008I is: 1262

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

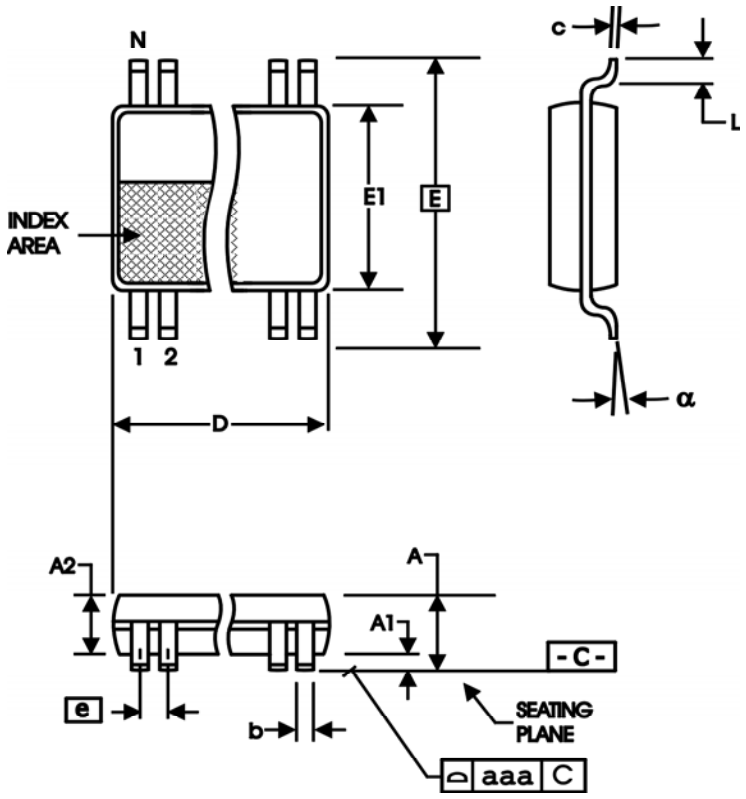


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MS-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87008AGI	ICS87008AGI	24 Lead TSSOP	tray	-40°C to 85°C
87008AGIT	ICS87008AGI	24 Lead TSSOP	1000 tape & reel	-40°C to 85°C
87008AGILF	ICS87008AGILF	24 Lead "Lead-Free" TSSOP	tray	-40°C to 85°C
87008AGILFT	ICS87008AGILF	24 Lead "Lead-Free" TSSOP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	14	Ordering Information Table - added "T" (for tape and reel) Part/Order Number.	9/10/04
A	T8	10 14	Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free part number, marking, and note.	2/21/06